

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,245	10/08/2003	Wolfgang M. J. Hofmann	Hofmann/Div	5667
23294	7590 12/16/2005		EXAMINER	
JONES, TULLAR & COOPER, P.C. P.O. BOX 2266 EADS STATION			CHACKO DAV	IS, DABORAH
	N, VA 22202		ART UNIT	PAPER NUMBER
			1756	

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/680,245	HOFMANN ET AL.				
Office Action Summary	Examiner	Art Unit				
	Daborah Chacko-Davis	1756				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on <u>08 Oe</u>						
· <u>-</u>	,					
• • • • • • • • • • • • • • • • • • • •	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4) ☐ Claim(s) 1-11 and 13-36 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-11 and 13-36 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) acce Applicant may not request that any objection to the of Replacement drawing sheet(s) including the correction 11) The oath or declaration is objected to by the Ex	epted or b) objected to by the Eddrawing(s) be held in abeyance. See ion is required if the drawing(s) is obj	e 37 CFR 1.85(a). ected to. See 37 CFR 1.121(d).				
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
Attachment(s)						
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) 	· _					
Paper No(s)/Mail Date <u>10/03</u> . 6) ☐ Other:						

Art Unit: 1756

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1-11, and 13-36, is rejected under 35 U.S.C. 102(b) as being anticipated by U. S. Patent No. 5,235,187 (Arney et al., hereinafter referred to as Arney).

Arney, in col 3, lines 52-67, in col 4, lines 1-51, in col 7, lines 60-67, in col 8, lines 1-40, in col 15, lines 1-30, in col 16, lines 14-29, in col 30, lines 12-23, discloses a micromachining process comprising forming a mask on the wafer (substrate), isotropically etching through the mask and undercutting the mask, thermally oxidizing the slightly under cut mask (passivating the substrate), alternately etching and thermally oxidizing (isotropically and anisotropically) the substrate to form a structure (has the geometry of the mask) in the substrate (isotropically undercutting), controlling the timing (based on etch rate, and deposition rate) of the etching and thermally oxidizing processes to produce vertical walls (deep trenches with vertical sidewalls), and adjusting the etch rate and oxidizing processes to produce increased thickness (higher oxidation rate), and completely under cut, by etching, and release the structure (claims 1, 13, 15, and 17). Arney, in col 3, lines 60-68, in col 4, lines 1-51, in col 29, lines 25-67, in col 30, lines 1-11, and in figure 13, discloses repeating the etching and oxidizing steps (low temperature) to produce a second released self-aligned structure below the

first structure in the substrate, and also forming features (high aspect ratio structure, see figure 18) using a single mask (claims 2, 11, 16, 18, 25). Arney, in col 8, lines 41-59, in col 29, lines 1-67, and in figure 13, discloses that the substrate is etched through the mask (recess etched through the mask) to form the first level structure having a first width, and further etching through the first level structure (trench etching process) to form the second level structure, followed by oxidation of the sidewalls of the trench resulting in the second level structure have a second width (sidewall thickness) greater than the first width, and then increasing the island height by etching (anisotropically, deep trench process) to release the second structure resulting in self aligned vertically stacked self-aligned structures (claims 3, 4, 22, 26-30). Arney, in col 7, lines 30-45, discloses that the structures (first and second) are electrically isolated (or insulated) by thermal oxidation, and providing electric leads (contacts) on selected points of the structure (claims 5, 6, 21, 23, 31-32). Arney, in col 29, lines 15-17, discloses forming an electrically conductive layer (polySi) on the structure (claims 7, 24, 33). Arney, in col 15, lines 1-20, discloses that the selected portions are etched using a focused ion beam (ion beam etching by direct writing) (claims 8, and 34). Arney, in col 29, lines 40-65, discloses that a selected portion of the structure is oxidized (all exposed area of the structure), followed by deep trench etching to etch away the oxidized portions to form the under cut (under cut the island portion) (claims 9, 35). Arney, in col 26, lines 65-67, in col 27, lines 1-20, discloses that a second nitride mask is formed on the structure,

followed by thermal oxidation of the masked structure (claims 10, 36). Arney, in col 4,

lines 42-55, in col 30, lines 16, discloses the etch and release of the structure without

Page 3

Application/Control Number: 10/680,245

Art Unit: 1756

further oxidation and etchback steps (claim 14). Arney, in col 9, lines 1-10, discloses that the substrate (released structure, tip structure) can be used in the formation of integrated circuit devices and can be electrically connected to capacitors, and can be used for sensing (claims 19-20).

Page 4

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daborah Chacko-Davis whose telephone number is (571) 272-1380. The examiner can normally be reached on M-F 9:30 - 6:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark F Huff can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

dcd

December 12, 2005.

MARK F. HUFF SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 1700